Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-10 (canceled)

11. (new): A method of reducing power consumption of a system having at least one processor, the processor being coupled to at least one queue which stores instructions for execution by the processor, the method comprising:

(a) analyzing at least one input;

(b) estimating the load of the system based, at least in part, on the analysis of step (a);

(c) determining a clock rate based, at least in part, on the estimation of step (b); and

(d) clocking the processor at the clock rate determined in step (c).

12. (new): The method of claim 11 wherein the input includes at least one instruction for processing by the processor.

13. (new): The method of claim 12 wherein the at least one instruction has a predetermined weight, the predetermined weight varying according to the type of the at least one instruction.

14. (new): The method of claim 13 wherein the estimation of step (b) changes based, at least in part, upon the predetermined weight.

15. (new): The method of claim 12 wherein the at least one instruction is generated in response to a user input.

16. (new): The method of claim 12 wherein the at least one instruction is generated automatically.

17. (new): The method of claim 16 wherein the at least one instruction is generated in response to the temperature of the processor.

18. (new): The method of claim 16 wherein the at least one queue includes a first instruction queue and a second instruction queue, and step (b) further comprises:

(b1) using a first group of instructions queued at the first instruction queue and a second group of instructions queued at the second instruction queue as separate control factors.

19. (new): A method of reducing power consumption of a system having at least one processor, the method comprising:

(a) analyzing at least one input;

(b) estimating a desired processing speed based, at least in part, on the analysis of step (a);

(c) determining a clock rate based on the estimation of step (b); and

(d) clocking the processor at the clock rate determined in step (c).

20. (new): A method of reducing power consumption of a system having at least one processor, the method comprising:

(a) analyzing at least one input;

(b) estimating a desired processing rate based, at least in part, on the analysis of step (a);

(c) determining a clock rate based on the estimation of step (b); and

(d) clocking the processor at the clock rate determined in step (c).

21. (new): A method of reducing power consumption of a system having at least one processor, the processor being in communication with at least one queue which stores instructions for execution, the method comprising:

controlling the clocking frequency of the processor in response to a prediction of the load of the system, the load being based, at least in part, on the instructions stored in the queue.

22. (new): The method of claim 21 wherein the at least one queue includes a first instruction queue associated with the processor.

23. (new): The method of claim 22 wherein the at least one queue further includes a second instruction queue associated with a second processor.

24. (new): The method of claim 21 wherein the prediction of load of the system is based on the complexity of the instructions stored in the at least one queue.

25. (new): The method of claim 24 wherein the prediction of the load of the system is based on the complexity of a subset of the instructions stored in the at least one queue.

26. (new): The method of claim 21 wherein the prediction of the load of the system is based, at least in part, on a subset of the instructions.

27. (new): The method of claim 21 wherein the prediction of the load of the system load includes a short term load prediction and a long term load prediction.

28. (new): The method of claim 27 wherein the short term load prediction is based on instructions likely to be executed in the short term.

29. (new): The method of claim 28 wherein the instructions likely to be executed in the short term are stored in a cache of the processor.

30. (new): The method of claim 27 wherein the long term prediction is based on instructions likely to be executed in the long term.

31. (new): The method of claim 30 wherein the instructions likely to be executed in the long term are stored in a cache external to said processor.

32. (new): A computer system comprising:

(a) at least one processor;

(b) at least one queue which stores instructions for execution by the processor;

(c) a clock electrically coupled to the processor; and

(d) a clock estimation device electrically coupled to the queue and the clock, the clock estimation device being configured to control the frequency of a clock signal output from the clock to the processor.

33. (new): The computer system of claim 32 wherein initially the processor runs at an initialization clock frequency, and subsequent clock frequencies are

determined by the clock estimation device based on the number instructions stored in the queue.

34. (new): The computer system of claim 33 wherein the subsequent clock frequencies are selected from a plurality of available clock frequencies.

35. (new): The computer system of claim 32 wherein the processor is a microprocessor.

35. (new): The computer system of claim 32 wherein the processor is a central processing unit (CPU).

36. (new): The computer system of claim 32 wherein the processor is a graphics processor.

37. (new): The computer system of claim 32 wherein the clock estimation device analyzes the types of instructions stored in the queue and assigns a weight to each one of the instructions based the intensity of processing required for the one instruction.

38. (new): The computer system of claim 32 further comprising:

(e) a temperature monitor device electrically coupled to the processor and the clock estimation device for maintaining the computer system at an acceptable range of operating temperature, wherein the clock estimation device factors in a temperature measured by the temperature monitor device.

39. (new): The computer system of claim 32 wherein the at least one queue comprises a memory buffer for queuing all instructions waiting to be executed by the processor, and an instruction cache for receiving the instructions from the memory buffer, queuing the received instructions and forwarding the instructions to the processor.

40. (new): A computer system comprising:

(a) a first processor;

(b) a first load and clock estimation device electrically coupled to the first processor;

(c) a second processor;

(d) a second load and clock estimation device electrically coupled to the second processor; and

(e) an instruction cache electrically coupled to the first and second processors and at least one of the first and second load and clock estimation devices, wherein the first and second load and clock estimation devices are synchronized.

41. (new): The computer system of claim 40 further comprising:

(f) a first clock electrically coupled to the first processor and the first load and clock estimation device; and

(g) a second clock electrically coupled to the second processor and the second load and clock estimation device, wherein the first load and clock estimation device is configured to control the frequency of a first clock signal output from the first clock to the first processor, and the second load and clock estimation device is configured to control the frequency of a second clock signal output from the first clock to the first processor.

42. (new): The computer system of claim 41 wherein when the first processor has a larger queued instruction backlog than the second processor, the frequency of the first clock signal and/or the second clock signal are adjusted to equalize the instruction backlog of the first and second processors.

43. (new): The computer system of claim 41 wherein when the first processor has a smaller queued instruction backlog than the second processor, the frequency of the first clock signal and/or the second clock signal are adjusted to equalize the instruction backlog of the first and second processors.

44. (new): The computer system of claim 40 further comprising:

(f) a memory buffer electrically coupled to the instruction cache and the first load and clock estimation device for queuing all instructions waiting to be executed by at least one of the processors.

45. (new): A computer system comprising:

(a) an optimum clock estimation device;

(b) at least one long term load estimation device electrically coupled to the optimum clock estimation device;

(c) at least one short term estimation device electrically coupled to the optimum clock estimation device;

(d) a clock electrically coupled to the optimum clock estimation device; and

(e) a processor electrically coupled to the clock, wherein each of the long term and short term load estimation devices analyze a set of instructions, and the optimum clock estimation device controls the frequency of a clock signal output from the clock to the processor based on at least one of the long term and short term analysis.